

Non Linear Response

Application Note

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Overview

The Zilker Labs Digital-DCTM devices incorporate a non-linear response (NLR) loop that decreases the response time and the output voltage deviation in the event of a sudden output load current step. The NLR loop incorporates a secondary error signal processing path that bypasses the primary error loop when the output begins to transition outside of the standard regulation limits. This scheme results in a higher equivalent loop bandwidth that what is possible using a traditional linear loop.

When a load current step function imposed on the output causes the output voltage to drop below the lower regulation limit, the NLR circuitry will force a positive correction signal that will turn on the upper MOSFET and quickly force the output to increase. Conversely, a negative load step (i.e. removing a large load current) will cause the NLR circuitry to force a negative correction signal that will turn on the upper MOSFET and quickly force the output to decrease. Refer to Figure 1.

There are three types of configuration setting variables utilized in the NLR: thresholds, time-outs and blanking. The following paragraphs explain how these settings affect the NLR response and the method for configuring them for optimum performance.

NLR thresholds

The thresholds are referred to as high side and low side, and can be set from 0.5% to 4.0% of the nominal output voltage in 0.5% steps.

When the output voltage crosses the high side threshold, the high side MOSFET (QH in Figure 3) is immediately turned on, and the low side MOSFET (QL) is turned off. This immediate change to the state of a MOSFET is referred to as a "correction". Since a high side threshold corresponds to an on-time correction to the high side MOSFET, the high side threshold is below the output voltage. Likewise, the low side threshold can be set from 0.5% to 4.0% above the nominal output voltage in 0.5% steps, and is independent of the setting of the high side threshold. In a similar fashion, if the low side threshold is exceeded, the low side MOSFET is immediately turned-on and the high side MOSFET is turned off.

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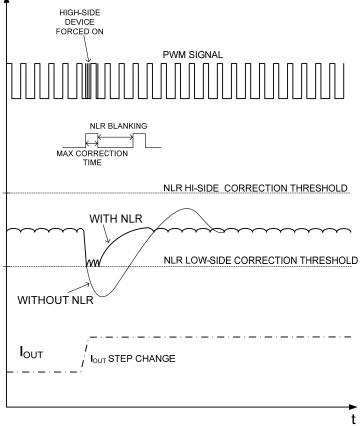


Figure 1. Non Linear Response (NLR)

The NLR thresholds are set with the NLR_CONFIG command and should be set 0.5% to 1.0% above the measured output voltage peak ripple and noise to avoid unintentional activation of NLR. Both the high side and low side thresholds have corresponding "outer" or higher/lower limits, and are set automatically to two times (2X) the high and low side thresholds respectively.

The use of outer thresholds is optional. The effectiveness of outer thresholds are evaluated by applying step loads with outer thresholds enabled and disabled and observing the resulting output voltage response on an oscilloscope. When any NLR threshold is exceeded, the correction continues until either the output voltage returns to within 0.25% of the nominal output voltage, called the hysteresis threshold, or the corresponding maximum correction time has expired.

Maximum Correction Time

The maximum high side and low side correction times are expressed as $1/64^{\text{th}}$ fractions of the total switching period ($1/f_{\text{SW}}$). The high side and low side correction times can be set from 1 to 7 of these $1/64^{\text{th}}$ switching period fractions independently.

<u>Blanking</u>

When an NLR correction has terminated, either due to a hysteresis threshold crossing or expiration of a correction time, a blanking timer is started. During a blanking time, corrections from the NLR are blocked and do not change the state of the top or bottom MOSFETs. Blanking time is set from 0 to 15 time units which are dependent on the voltage across the output inductor, V_L. For high side corrections, V_L is Vin -Vout and for low side corrections V_L is Vout. The blanking time units are V_L times 1/64th fractions of the total switching period $(1/f_{sw})$. A minimum blanking time is set by the controller IC and is equal to the current sensing delay time. The default current sense delay time is 254 ns for DCR sensing (using the inductor's parasitic resistance as a current sensing element and 672 ns when using R_{DS(on)} sensing (using QL as the current sensing element).

Setting Correction and Blanking times

The NLR parameters are set using the NLR_CONFIG command. Figure 2 shows nominal NLR settings for the ZL2005.

In general, blanking time can be left at zero since the device has minimum default blanking times as

described above. As with outer thresholds, correction and blanking times are optimized by experimentation.

Parameter	Range	Units	
High Side Threshold	0.5 to 4.0	% of V_{OUT}	
Low Side Threshold	0.5 to 4.0	% of V _{OUT}	
High Side Max Correction Time	1, 3, 5, 7	X T _{SW} /64	
Low Side Max Correction Time	1, 3, 5, 7	X T _{SW} /64	
Blanking Control	0 - 15	X V _L X T _{SW} /64	

Table 1. NLR Parameters

After setting suitable high and low side thresholds, start with a correction time of 1 and a blanking time of 0. Apply the maximum expected load step and observe the output voltage response. The output voltage should settle back within the desired regulation band within 2 or less opposite NLR excursions in the polarity opposite the initial output voltage deviation, also referred to as overshoot. More than 2 overshoots will cause an excessive increase in the effective switching frequency and could lead to a reduction in overall power supply efficiency. Continue to increase the correction time with a corresponding increase in blanking until a balance is met between improved transient response and number of overshoots. Likewise, reduce the blanking time to optimize transient response and minimize overshoots. Finally, test the NLR settings over input voltage and output step current variations to verify that the desired performance has been achieved.

NLR Enable Outer Threshold Enable	>	
High Side Threshold	1.5	% of VOUT
Low Side Threshold	1.5	% of VOUT
Hi Side Max Correct Time	3	"Tsw/64
Lo Side Max Correct Time	3	*Tsw/64
NLR Blanking Control	0	*VL*Tsw/64
NLR_CONFIG	4250	

Figure 2. Nominal Settings for ZL2005

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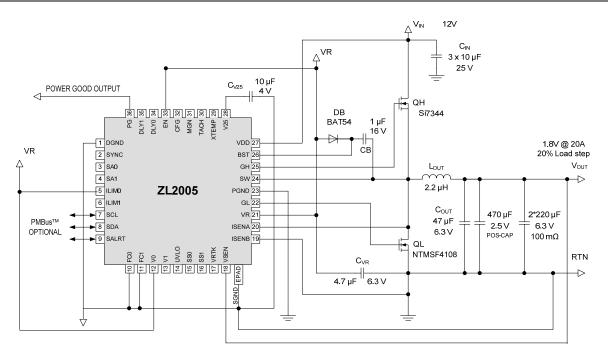


Figure 3. Typical Application Circuit



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